

The block diagram illustrates the system architecture. It consists of three main components connected in a linear sequence:

- 12 TARGET PROCESSOR**: The leftmost component, represented by a rectangular box.
- 14**: A bidirectional arrow connecting the Target Processor (12) to the Emulation Unit (11).
- 11 EMULATION UNIT**: The central component, represented by a rectangular box.
- 15**: A bidirectional arrow connecting the Emulation Unit (11) to the Host Processing Unit (10).
- 10 HOST PROCESSING UNIT**: The rightmost component, represented by a rectangular box.

The components are labeled with their respective reference numerals (10, 11, 12, 14, 15) above them.

FIG. 1B

The diagram illustrates the internal structure of the trigger generation unit. On the left, a large box labeled **MONITORING AP** (18) contains a vertical stack of **EVENT SIGNAL GENERATION UNIT** blocks, labeled 18₁ through 18_N. Each of these units receives an external input and outputs an **EVENT SIGNAL**. These event signals are fed into a central **TRIGGER GENERATION UNIT**. This unit processes the event signals and produces multiple **TRIGGER SIGNALS**, which are shown as a group of outputs on the right.

FIG. 2

FIG. 3

